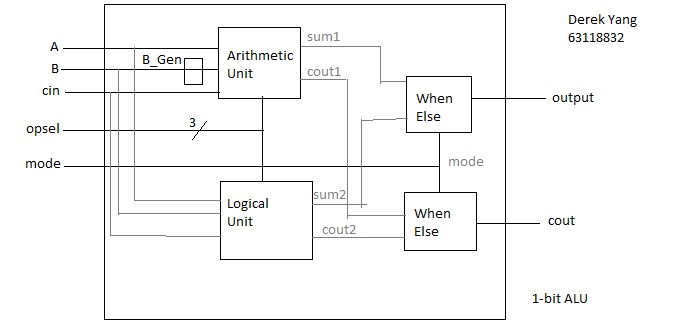
Arithmetic Logical Unit:

This unit is a combination of a 1-bit arithmetic and logical unit. This circuit takes an initial input A and B and preforms different operations depending on the mode selected and the operation selection code. There are in total 7 arithmetic operations that the arithmetic unit is responsible for running and 5 logical operations that the logical unit is responsible for running. When the mode is 0, the arithmetic unit connects to the output and when the mode is 1, the logical unit connects through to the output.

Circuit Design:



Truth Table:

B\_Generator:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| b | s2 | s1 | s0 | b\_gen |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| b | s2 | s1 | s0 | b\_gen |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | X |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | X |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | X |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | X |

K-Map:

B\_Generator

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| s1s0/  Bs(2) | 00 | 01 | 11 | 10 |
| 00 |  | 1 | 1 | X |
| 01 |  | 1 | X |  |
| 11 |  | 1 | X | 1 |
| 10 | 1 |  |  | X |

Boolean Equations:

Arithmetic Unit:

Output = A XOR B\_Gen XOR cin

B\_Gen = (opsel(0) x B’) + (opsel(2) x opsel(0)) + (B x opsel(2)’ x opsel(0)’) + (B x opsel(2) x opsel(0)’)

Cout = (A x B\_Gen) + (A x cin) + (B\_Gen x cin)

Logical Unit:

Output =

{

A AND B,

A OR B,

A XOR B,

NOT A,

cin

}

Wave Map

